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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/452,691	12/02/1999	FRED D. BAILEY	TI-27935	1638

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/452,691	BAILEY ET AL.	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication app ars on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8 and 17-20* is/are rejected.

7)☒ Claim(s) *4 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first plurality of conductively filled vias extending from said upper metal interconnect layer to said lower interconnect layer of claims 18 and 20 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 18 and 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically, the specification and drawings do not disclose a first plurality of conductively filled vias extending from said upper metal interconnect layer to said lower interconnect layer.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Keil et al. (U.S. Patent No. 5,541,442).

In re claims 1, 17 and 19, Keil (Fig. 1) discloses a semiconductor device, comprising:

A lower metal interconnect layer ((30) located over a semiconductor body (12);

A multi-level dielectric (28, 40) layer located over said lower interconnect layer;

An upper metal interconnect layer (46) located over said multi-level dielectric layer; and

A thin film resistor (38) embedded within said multi-level dielectric layer between said lower metal interconnect layer and said upper metal interconnect layer, wherein said thin film resistor comprises a resistor layer that is physically separated, in its entirety, in a vertical direction from any metal interconnect layer.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 17 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishikawa et al. (U.S. Patent No. 5,751,050).

In re claims 1, 17 and 19, Ishikawa (Fig. 8) discloses a semiconductor device, comprising:

A lower metal interconnect layer (81) located over a semiconductor body (70);

A multi-level dielectric (71, 76) layer located over said lower interconnect layer;

An upper metal interconnect layer (82) located over said multi-level dielectric layer; and

A thin film resistor (73) embedded within said multi-level dielectric layer between said lower metal interconnect layer and said upper metal interconnect layer, wherein said thin film resistor comprises a resistor layer that is physically separated, in its entirety, in a vertical direction from any metal interconnect layer.

In re claim 2, Ishikawa discloses the device of claim 1, further comprising:

A first via (79) extending from said upper metal interconnect layer to said lower interconnect layer; and

A second via (78) extending from said upper metal layer to said thin film resistor.

In re claim 3, Ishikawa discloses the device of claim 1, wherein said thin film resistor comprises a hard mask (76) located over an end of the thin film resistor. Note that Ishikawa denotes the layer (76) as a silicon oxide, but does not expressly explain that said layer could be a hard mask. Shen et al. (U.S. Patent No. 6,627,971 B1) is included here as a teaching reference to show that silicon oxide (14) has specific use as a hard mask (Shen; column 3, lines 3-4).

Claims 17 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Saia et al. (U.S. Patent No. 5,874,770).

In re claim 17, Saia discloses a semiconductor device, comprising:

A lower metal interconnect layer (46) located over a semiconductor body (45);

A multi-level dielectric layer (42, 10, 40) located over said lower interconnect layer;

An upper metal interconnect layer (47) located over said multi-level dielectric layer; and

A thin film resistor (28) embedded within said multi-level dielectric layer between said interconnect layer and said upper metal interconnect layer.

In re claim18, Saia discloses the device of claim17, further comprising:

A first plurality of conductively filled vias (47) extending from said upper metal interconnect layer to said lower interconnect layer; and

A second plurality of conductively filled vias (21, 52) extending from said upper metal layer to said thin film resistor.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa as applied to claim 1 above, and further in view of Redford et al. (U.S. Patent No. 6,081,014).

In re claim 6-8, Ishikawa discloses the device of claim 1, but does not expressly disclose the thin-film resistor comprising TaN, SiCr or NiCr. Redford discloses the use of thin-film resistor materials including polysilicon, silicon chrome, nichrome and tantalum (column 1, lines 23-28). It would have been obvious for one skilled in the art to use silicon chrome, nichrome, or tantalum as disclosed by Redford for the resistor structure of Ishikawa for the purpose, for

example, of enhancing the performance of the resistor based on its resistance, tolerance, or TCR (Redford, column 1, lines 29-35).

Allowable Subject Matter

6. Claims 4 and 5 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

8. Applicant's arguments filed 11/08/03 have been fully considered but they are not persuasive.

a. In re claim 17, Applicant argues (Remarks/Arguments, pp. 7) that Saia does not disclose or suggest the claimed thin film resistor being in a semiconductor chip of an IC; that the flexible interconnect film is part of an external circuit to the chip (44). In response, Examiner points out similar language in claim 17 to the disclosure of Saia. Claim 17 recites that the "lower interconnect layer" is located *over* a semiconductor body. This is the same relationship the interconnect film of Saia has to the semiconductor body. That is, the interconnect electrodes and the thin-film resistor in both disclosures lay *above* the semiconductor body. The interconnect structure of the

claimed invention is as much formed external to the integrated circuit chip as the interconnect of Saia.

b. Secondly, if the interconnect structure of Saia is formed external to the semiconductor body, such a configuration does not preclude the entire device being interpreted as an integrated circuit. Those skilled in the art will recognize that any number of layered devices atop a semiconductor substrate generally combine with the substrate to collectively form "integrated circuits." There are few semiconductor integrated circuit devices in which the entire device is comprised solely of the semiconductor substrate. Most devices have several layers of interconnects, dielectric layers, and other materials between the substrates and external connections that comprise the total "integrated circuit."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 703-308-8137. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Jesse A. Fenty Jesse A. Fenty

Examiner
Art Unit 2815

JAF